Master Thesis

Ultra-low power programmable processor architecture for 60 GHz digital front-end

Προγραμματιζόμενη αρχιτεκτονική επεξεργαστών πολύ χαμηλής κατανάλωσης για ψηφιακό front-end στα 60 GHz

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NUMBER OF MASTER THESIS ........../2011

May 2011
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May 2011
Acknowledgements

The present master thesis, entitled: "Ultra-low power programmable processor architecture for 60 GHz digital front-end", is the research work carried out during the Master of Science program "Integrated Systems of Hardware and Software" of the Department of Computer Engineering and Informatics of the Polytechnic Faculty of University of Patras. The study has been conducted in cooperation with the Interuniversitair Micro-Elektronica Centrum (IMEC) and University of Patras. The assignment and supervision of the present study has been done by the Professor of Electrical and Computer Engineering Department of the University of Patras Prof. Constantinos Goutis, whom I warmly thank for motivating push my limits further and explore new fields of knowledge.

I thank IMEC for its cooperation with me and for offering access to its facilities in Leuven, Belgium. During my stay in Leuven Professor Francky Catthoor has contributed a decisive role not only in the development and completion of my work but also for my way of thinking. I express my deep appreciation for his guidance during these six months that helped me surpass all the problems that I encountered on my way and helped me have a deeper understanding of my subject. He has been a mentor for me all these six months abroad.

Special thanks I would like to express to my team members at the IMEC Leuven site, Wim Van Thillo, Robert Fasthuber and Praveen Raghavan for their valuable and vital contribution to the completion of this study. Moreover, special thanks David Novo Bruna, post-doc to EPFL, without his invaluable help and guidance this thesis would have been impossible.

In closing, I thank the Professor Dr. Georgios Theodoridis of the Department of Electrical and Computer Engineering Department of the University of Patras and the Professor Dr. Dimitrios Nikolos of the Department of Computer Engineering and Informatics Department of the University of Patras, who form, together with the supervisor Dr. Constantinos Goutis, the committee of my master thesis.
This study would not have been completed without the full moral support, throughout my postgraduate studies, of people that are standing close to me. This is especially so for Stephanie and her constant support through all the time that I worked on this work. Also for my family, and as a minimum return I sincerely thank them. I dedicate my master thesis to my beloved parents, Xarilaos and Ifigeneia, and brother, Vasilis.

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Patras, May 2011
Ελληνική περίληψη διπλωματικής εργασίας

Τα σύγχρονα ηλεκτρονικά συστήματα παρέχουν στους χρήστες έναν καθημερινά αυξανόμενο αριθμό υπηρεσιών και λειτουργιών. Η ζήτηση της αγοράς για φθηνές, αξιόπιστες και φορητές ηλεκτρονικές συσκευές απειλεί τα όρια του σχεδιασμού των ενσωματωμένων συστημάτων σε νέες ανεξερεύνητες περιοχές. Η φορητότητα απαιτεί την αφαίρεση όλων των καλώδιων είτε για μετάδοση δεδομένων είτε για ενέργεια. Για να επιτευχθεί αυτό, η ασύρματη επικοινωνία σε υψηλό ρυθμό μετάδοσης είναι επιθυμητή χαράς να θυσιαστεί η υψηλή ενεργειακή αποδοτικότητα που καθιστά την συσκευή αυτόνομη από το ενεργειακό δίκτυο για μεγάλες χρονικές περιόδους. Η συνεχής αύξηση στις προ-διαγραφές των σύγχρονων ενσωματωμένων συστημάτων έχει οδηγήσει στην χρήση καινοτόμων ιδεών, προσεγγίσεων και τεχνολογιών.

Εισαγωγή στις ασύρματες επικοινωνίες στα 60 GHz

Μια νέα τεχνολογία που υπόσχεται υψηλή ολοκλήρωση και υψηλό ρυθμό μετάδοσης δεδομένων στις ασύρματες ζεύξεις είναι η επικοινωνία στα 60 GHz. Η επικοινωνία στα 60 GHz έχει κάποια πλεονεκτήματα καθώς και μερικά μειονεκτήματα. Αυτά αναφέρονται παρακάτω όπως στο [29].

Τα βασικά πλεονεκτήματα είναι:

1. Η παγκόσμια διαθεσιμότητα του εύρους ζώνης είναι τεράστια. Η εικόνα 1 δείχνει μια σύγκριση μεταξύ των 60 GHz, IEEE 802.11 WLAN και ultra-wideband (UWB) συστήματα. Τα 60 GHz προσφέρουν ξεκάθαρα πρωτοφανείς δυνατότητες.

2. Επιπλέον, η μεγάλες απώλειες μονοπατίου και η υψηλή εξασθένηση σε τοίχους συνεπάγει κάποια πλεονεκτήματα. Πρώτον, ότι επιτρέπουν την επαναχρησιμοποίηση συχνοτήτων σε μικρές αποστάσεις. Δεύτερον ότι το φαινόμενο multipath είναι λιγότερο επιθετικό.

3. Τέλος, οι δυνατότητες σμίκρυνσης των αναλογικών στοιχείων - λόγω του γεγονότος ότι το μήκος κύμματος στον ανοιχτό χώρο είναι μόλις 5 mm - είναι ένα σαφές πλεονέκτημα των 60 GHz.
Σχήμα 1: Σύγκριση εύρους ζώνης IEEE 802.11, UWB και 60 GHz συστημάτων

Σε αντίθεση με τα παραπάνω υπάρχουν μερικά μειονεκτήματα:

1. Οι μεγάλες απώλειες μονοπατιού στα 60 GHz σημαίνουν ότι θα πρέπει να χρησιμοποιηθεί ένα πολύ περιορισμένο προϋπολογισμό ζεύξης (link budget). Η μειωμένη ενίσχυση των CMOS transistor στις συχνότητες αυτές περιορίζει τον προϋπολογισμό ακόμα περισσότερο.

2. Λόγω του υψηλού μετάδοσης δεδομένων ακόμα πιο υψηλές προδιαγραφές απαιτούνται για τα αναλογικά στοιχεία όπως μετατροπείς αναλογικού σήματος σε ψηφιακό σήμα πολλών Gsamples/s.

3. Τέλος, μη ιδανικές καταστάσεις του καναλιού έχουν πολύ μεγαλύτερες επιπτώσεις από ότι στις επικοινωνίες χαμηλότερων συχνοτήτων.

Η παγκόσμια διαθεσιμότητα, υψηλή μετάδοση δεδομένων και οι δυνατότητες ολοκλήρωσης καθιστούν την τεχνολογία της επικοινωνίας στα 60 GHz σημαντική για μελλοντικές ασύρματες εφαρμογές. Αυτός είναι ο κύριος λόγος που μας κινητοποιεί να εξερευνήσουμε την αρχιτεκτονική του υλικού των στοιχείων της ψηφιακής της βάσης.
Αλλά η ψηφιακή μεριά του δέκτη στα 60 GHz πρέπει να λειτουργεί σε πολύ υψηλούς ρυθμούς μετάδοσης δεδομένων, που σημαίνει ότι θα καταναλώνει επίσης ένα μεγάλο ποσό ενέργειας. Για μια συσκευή που λειτουργεί με μπαταρία αυτό δεν είναι αποδεκτό και για αυτόν τον λόγο έξυπνης, λιγότεροι συμβατοί τρόποι που θα μειώσουν ξανά την κατανάλωση ενέργειας είναι αναγκαίοι. Για αυτόν τον σκοπό έξυπνο εξερευνούμε μια πρόοπτη καινοτόμη ιδέα με την οποία μπορούμε να εκμεταλευτούμε τον διαθέσιμο δυναμισμό που είναι έμμονα παράστη την ροή των δεδομένων που παρέχεται στα στοιχεία του ψηφιακού front end των 60 GHz.

Η ιδέα των Σεναρίων Συστήματος - System Scenarios

Μια νέα προσέγγιση σχεδιασμού για ενσωματωμένα συστήματα υπό-σχετικά αποτελεσματική εκμετάλευση του δυναμισμού που μπορεί να παρουσιάζει ένα σύστημα. Τα αυτόματα συστήματα επικοινωνιών λειτουργούν τυπικά σε πολύ δυναμικό περιβάλλον. Τα Σενάρια συστήματος [15] έχουν μεγάλες δυνατότητες για να βελτιώσουν την αποτελεσματικότητα της υλοποίησης των ψηφιακών βάσεων συστημάτων.

Η βασική ιδέα πίσω από τα Σενάρια Συστήματος είναι η κατηγοριοποίηση του συστήματος από μια προοπτική κόστους κατά την διάρκεια σχεδιασμού και η εκμετάλευση της κατηγοριοποίησης κατά την διάρκεια της λειτουργίας. Στην παρούσα διπλωματική προσπαθούμε να εφαρμόσουμε την μεθοδολογία σχεδιασμού των Σεναρίων Συστήματος για να βελτιώσουμε την υλοποίηση ενός στοιχείου FFT (Fast Fourier Transform - Γρήγορος Μετασχηματισμός Φουριέ) που βρίσκεται στο μέρος του δέκτη στο μέρος της εξίσωσης στο πεδίο των συχνοτήτων (Frequency Domain Equalization). Η βασική ιδέα είναι να κατηγοριοποιήσουμε τα διάφορα στιγμήντα του FFT (που ονομάζονται καταστάσεις πραγματικού χρόνου - real time situations - RTS) από μια προοπτική κόστους, στην περίπτωση μας τον αριθμό των bits που χρειάζονται για να αναπαραστεί κάθε σήμα του FFT, και να χρησιμοποιήσουμε διαφορετικά σχέδια κατηγοριοποίησης κατά την διάρκεια λειτουργίας για να μειώσουμε αποτελεσματικά την κατανάλωση του στοιχείου.
Τυπικά, για να αντιμετωπιστεί η αυξανόμενη πολυπλοκότητα των σύγχρονων ενσωματωμένων συστημάτων, ένα σύστημα συνήθως διαιρείται σε διαφορετικές περιπτώσεις χρήσης (use cases). Μια use case καθορίζεται από τον σχεδιαστή από μια οπτική γωνία χρήσης. Κατά την διάρκεια λειτουργίας καθορίζεται από τον χρήστη κατά την αλληλεπιδρασή του με την εφαρμογή. Σε αντίθεση, ένα Σενάριο Συστήματος χαρακτηρίζεται από κάποια λειτουργία και καθορίζεται από μια οπτική γωνία χρήσης πόρων. Κατά την λειτουργία τα Σενάρια Συστήματος αντιπροσωπεύουν ένα ανιχνεύσιμο σύνολο λειτουργικών καταστάσεων μιας αντιστοιχισμένης (mapped) εφαρμογής, που είναι όμοιες από πλευράς κόστους πάνω στην επιλεγμένη πλατφόρμα. Στην εικόνα 2 φαίνεται πως η μεθοδολογία των Σεναρίων Συστήματος ενσωματώνεται στην παραδοσιακή μεθοδολογία σχεδιασμού των ενσωματωμένων συστημάτων.

Σχήμα 2: Ενσωμάτωση της μεθοδολογίας σχεδιασμού των Σεναρίων Συστήματος στην παραδοσιακή ροή σχεδιασμού των ενσωματωμένων συστημάτων.

Με αυτόν τον τρόπο μπορούμε να εκμεταλευτούμε τον δυναμισμό που εμφανίζεται σε διάφορες παραμέτρους ενός συστήματος προσθέ-
τονίσεις ένα μικρό υπερκέιμενο κόστος λόγω της εναλλαγής μεταξύ
dιαφορετικών Σεναρίων Συστήματος κατά την διάρκεια της λειτουρ-
γείας. Ωστόσο, το επιπλέον κόστος υπερκαλύπτεται από το κέρδος του
dυναμισμού. Τα Σενάρια Συστήματος έχουν εφαρμοστεί στο παρελ-
θόν εκμεταλευόμενα μεταβλητές ελέγχου με μεγάλη επιτυχία, μερι-
κές αναφορές μπορούν να βρεθούν στα: [28], [11], [12], [13], [14], [18]
και [24]. Στην παρούσα διπλωματική ουσία προσπαθούμε να εφαρ-
μόσουμε τα Σενάρια Συστήματος χρησιμοποιώντας μεταβλητές δεδο-
mένων ως παραμέτρους για να δημιουργήσουμε διαφορετικά Σενάρια
Συστήματος. Αυτή η εφαρμογή έχει περισσότερες δυνατότητες εφαρ-
mογής αλλά οι προκλήσεις για την ορμοθμοποίηση και την ανίχνευση
είναι μεγάλες. Για να κάνουμε εφικτή την χρήση των Σεναρίων Συ-
στήματος κατά την λειτουργία, επιχειρούμε να εκμεταλευτούμε τον
dυναμισμό των απαιτήσεων κβαντοποίησης για τα δεδομένα στη ροή
dεδομένων.

Πρόβλημα κβαντοποίησης

Όταν ένα αναλογικό σήμα αναπαρίσταται σε ψηφιακή μορφή μια
απώλεια στην ακρίβεια του σήματος είναι αναμενόμενη λόγω κβαν-
tοποίησης. Το πρόβλημα είναι ότι η ψηφιακή αναπάρασταση ενός
σήματος περιορίζεται από πεπερασμένη ακρίβεια σε αντίθεση με την
άπειρη ακρίβεια του αναλογικού ισοδύναμου. Οι σχεδιαστές συστη-
mάτων αντιμετωπίζουν αυτή τη διαπραγμάτευση μεταξύ του θορύβου
κβαντοποίησης που εισάγεται λόγω της έλλειψης ακρίβειας και τον
αριθμό των bits που χρειάζονται για να αναπαραστήσουν ένα σήμα
αυξάνοντας το κόστος του συστήματος.

Τα σήματα είναι αναπαραστάσεις φυσικών ποσοτήτων όπως η θερ-
μοκρασία, η πίεση, η τάση, η φωτεινότητα κλπ. Τα περισσότερα σή-
ματα του φυσικού κόσμου είναι αναλογικής φύσεως που σημαίνει
ότι αλλάζουν συνεχώς στο χρόνο και στο πλάτος τους. Η μετάδοση
tους μέσω ψηφιακών τεχνικών, που είναι ουσιαστικά διακριτές, απαι-
tετει κβαντοποίηση. Έτσι, οι επιδράσεις της κβαντοποίησης είχαν ρε-
λετηθει ενεργά για περισσότερα από πενήντα χρόνια όπως αναφέρεται
στο [22].

Ο πρωταρχικός σκοπός της κβαντοποίησης είναι να βρεθεί ένα συμ-
παγές σχέδιο που αντιπροσωπεύει την πηγαία πληροφορία αποτε- 
λευκισμικά και αξιόπιστα ([16]). Νέες επιδράσεις της κβαντοποίησης εμφανίστηκαν στις αρχές του 1970 λόγω της άνθισης της ψηφιακής επεξεργασίας σήματος ([23]). Ο αντικειμενικός σκοπός εδώ είναι η κατανόηση του πώς η πεπερασμένης ακρίβειας επεξεργασία σήματος διαφέρει από την επεξεργασία σήματος άπειρης ακρίβειας για ένα ψη- 
φιακό διακριτού χρόνου συστήματος ψηφιακής επεξεργασίας. Είναι σημαντικό να διαχωριστούν αυτά τα δυο θέματα στην βιβλιογραφία.

Η σχετική βιβλιογραφία υποθέτει δυαδικά αριθμητικά συστήματα στα-
θερής υποδιαστολής (fixed-point) με είτε στρογγυλοποίηση ή απο-
κοπή ως μέσο κβαντοποίησης ([22]). Γενικά υπάρχει συμφωνία στον 
διαχωρισμό της ανάλυσης των στατικών δεδομένων σε δυο βήματα: 
ανάλυση εύρους και ανάλυση ακρίβειας. Η ανάλυση εύρους παρέχει 
το περιθώριο να εξυπηρετηθούν η αύξηση των δεδομένων (αποφεύγο-
ντας την υπερχείληση), ενώ η ανάλυση ακρίβειας εγγυάται την ακρίβεια 
της λειτουργίας. Όμως διαφορετικές προσπεχρικές έχουν ακολουθηθεί 
για τις αναλύσεις εύρους και ακρίβειας.

Όλες οι μέθοδοι της βιβλιογραφίας αντιμετωπίζουν δυσκολίες είτε σε 
μεγάλους χρόνους εξομοίωσης είτε σε μεγάλους περιορισμούς στα χα-
ρακτιστικά του εξεταζόμενου συστήματος. Η μέθοδος που παρου-
σιάζεται στο [6] ξεπερνά τα περισσότερα από αυτά τα προβλήματα και 
παριγράφει μια πιο γενική και υψηλά κλιμακώμενη προσέγγιση στο 
πρόβλημα της κβαντοποίησης. Ωστόσο ακόμα έχει προβλήματα στους 
χρόνους υπολογισμών όταν μεγάλα αλγοριθμικά κομμάτια με συμπε-
ριθυρία συνδιασμένων πολλαπλασιασμών και πρόσ- θες ψηφιο-
ται. Αυτό συμβαίνει για παράδειγμα με την περίπτωση του κομματιού 
του ΦΤ. Έτσι, στην παρούσα διπλωματική εργασία επεκτείνουμε την 
μέθοδο αυτή με ένα σημαντικό νέο βήμα για να αφαιρέσουμε αυ-
τή την αδυναμία. Χρησιμοποιούμε την τροποποιημένη μέθοδο για 
να παράγουμε διαφορετικά σχέδια κβαντοποίησης για κάθε Σενάριο 
Συστήματος του ΦΤ. Αυτά μπορούμε να τα εκμεταλευτούμε κατά 
την λειτουργία όταν ένα διαφορετικό στιγμιότυπο του ΦΤ ανιχνεύ-
ται. Αλλά για να επιτευχθεί η εκμετάλευση του μεταβλητού μήκους 
λέξης που παράγεται για το σύστημα χρειαζόμαστε ένα κατά-
ληπή επεξεργαστική πλατφόρμα όπου η δυναμική αλλαγή των μηκών 
λέξης προκαλούν μεγάλες αλλαγές στις ενεργειακές απαιτήσεις. Αυτό 
επιτυγχάνεται με την εκμετάλευση της επονομαζόμενης Soft-SIMD
Οι Single Instruction Multiple Data (SIMD) εντολές χρησιμοποιούνται για την αύξηση της απόδοσης των εφαρμογών, καθώς εκτελούν, την ίδια χρονική στιγμή, μια εντολή σε ένα διάνυσμα από διαφορετικά δεδομένα. Οι SIMD εντολές εκμεταλεύονται τον παραλληλισμό δεδομένων που περιέχεται σε εφαρμογές όπως η multimedia. Μπορεί να εκτελεστεί χρησιμοποιώντας είτε hardware είτε software.

Σχήμα 3: Εφαρμογή των SIMD εντολών. Αντί για έναν τελεστή για ένα δεδομένο μικρού μήκους λέξης, διαφορετικά δεδομένα συνδιάζονται σε μια μεγάλη λέξη.

Οι Hardware-SIMD (Hard-SIMD) εντολές (εικόνα 4) χρησιμοποιείται από ενεργειακά αποδοτικούς επεξεργαστές υψηλής απόδοσης που παρέχουν ειδικό υλικό στο data path τους για να υποστηρίζουν συνδιασμούς υπολέξεων (subwords) με το ίδιο μήκος, π.χ. 1x64bits, 2x32bits, 4x16 bits ή 8x8 bits. Ο περιορισμένος αριθμός υπολέξεων θέτουν το όριο των δεδομένων στην επόμενη διαθέσιμη δύναμη του δυο, που οδηγεί σε μια χρησιμοποιούμενα bits και κατ'επέκταση σε απόλεια απόδοσης. Επιπλέον, διαφορετικές Hard-SIMD υλοποιήσεις είναι μη συμβατές μεταξύ τους, λόγω του γεγονότος ότι κάθε υλοποίηση παρέχει έναν αριθμό SIMD εντολών και ένα σετ από εντολές πακεταρίσματος και ξεπακεταρίσματος βασισμένες σε μια συγκεκριμένη αρχιτεκτονική οδηγώντας σε μικρή μεταφερσιμότητα της εφαρμογής.

Οι Software SIMD (Soft-SIMD) εντολές (εικόνα 5) είναι ανεξάρτητες από την αρχιτεκτονική παρέχοντας μεταφερσιμότητα της εφαρμογής. Οι Soft-SIMD εντολές δεν απαιτούν συγκεκριμένη υποστήριξη υλικού και ως αποτέλεσμα, επιπλέον εντολές μπορούν να προστεθούν πλατφόρμας που περιγράφεται παρακάτω.
Σχήμα 4: Hardware SIMD με 16 bits υπολέξεις.

(Σχήμα με 16 bits υπολέξεις)

για να εξασφαλίσουν την ορθότητα λειτουργίας. Έτσι, η αύξηση της απόδοσης των Soft-SIMD εντολών είναι μικρότερη σε σχέση με αυτή των Hard-SIMD αλλά λόγω της ευκαμψίας των υπολέξεων μπορούν να εξερευνήσουν τις πληροφορίες σχετικά με τα μήκη λέξεων κάνοντας πιο αποδοτικούς συνδιασμούς. Αυτή την ευκαμψία προσπαθούμε να εκμεταλευτούμε παράγοντας περισσότερα από ένα σχέδια κβαντοποιήσης για κάθε στοιχείο υλικού.

Σχήμα 5: Software SIMD με διαφορετικά μήκη υπολέξεων.

(Σχήμα με διαφορετικά μήκη υπολέξεων)

ης του FFT χρησιμοποιώντας διαφορετικά σχέδια κβαντοποίησης. Εφ’όσον η ομαδοποίηση των πράξεων οδηγεί σε λιγότερες πράξεις, υποθέτουμε ότι η μείωση στον αριθμό των bits που χρειάζονται για την αναπαράσταση των εσωτερικών σημάτων του FFT είναι άμεσα συνδεδεμένο με την κατανάλωση ενέργειας του στοιχείου. Έτσι στηρίζομε στο συνδυασμό της ιδέας των Σενάριων Συστήματος και τα διαφορετικά σχέδια κβαντοποίησης, προσπαθούμε να καταλήξουμε με μια πιο ενεργειακά αποδοτική υλοποίηση του στοιχείου κάτω από δυναμικές συνθήκες.

Συνεισφορά της παρούσας διπλωματικής εργασίας.

Στην παρούσα διπλωματική εξερευνούμε της δυνατότητες της αρχιτεκτονικής του FFT που βρίσκεται στην πλευρά του δέκτη ενός πομποδέκτη στα 60 GHz. Ο FFT είναι μέρος της εξίσωσης στο πεδίο της συχνότητας που χρησιμοποιείται για να μειώσει της επιδράσεις του φαινομένου multipath. Χρησιμοποιώντας Σενάρια Συστήματος προσπαθούμε να καταλήξουμε με μια πιο προσαρμοστική και συνεπώς πιο ενεργειακά αποδοτική υλοποίηση του μετασχηματισμού. Η εφαρμογή των Σενάριων Συστήματος της κβαντοποίησης δεδομένα ως παράμετρο είναι μια καινοτόμα προσέγγιση και σε αυτή την διπλωματική εργασία ελέγχουμε την επιτυχία της. Για να επιτύχουμε κάτι τέτοιο πρέπει να μπορούμε να παράγουμε πολλαπλά διαφορετικά σχέδια κβαντοποίησης του μετασχηματισμού σε αποδεκτά χρονικά διαστήματα. Οι παρούσες μεθόδους κβαντοποίησης δεν μπορούν ακόμα να παρέχουν τέτοια δυνατότητα. Έτσι βασίζομε στην επέκταση μια υπάρχουσας μεθοδολογίας προτείνουμε μια ολοκληρωμένη μεθοδολογία που μπορεί να παράγει σχέδια κβαντοποίησης μεγάλων στοιχείων υλικού όπως ο FFT.

Συμπεράσματα

Με την τροποποίηση της υπάρχουσας μεθοδολογίας κβαντοποίησης καταφέραμε να μειώσουμε τον χρόνο υπολογισμού ενός σχεδίου κβαντοποίησης του FFT από 17.500 ώρες σε μόλις 2 ώρες. Αυτό είχε ως κό-
στος την μείωση της καταλληλότητας των αποτελεσμάτων αλλά ακόμα και με την τροποποιημένη μεθοδολογία καταφέραμε να μειώσουμε τον αριθμό των bits των σημάτων του μετασχηματισμού κατά 75%.

Επιπλέον, ο πειραματισμός με διαφορετικές ομαδοποιήσεις των στιγμιότυπων του FFT κατέλειξε σε σημαντικά συμπέρασμα όσο αναφορά τις ανάγκες των σημάτων του σε bits και τον συσχετισμό των δεδομένων στις εισόδους του καθώς και στις ενδοιάμεσες βαθμίδες του. Ως αποτέλεσμα με την εφαρμογή των Σεναρίων Συστήματος βασισμένον σε παραμέτρους δεδομένων, μια καινοτόμα προσέγγιση, καταφέραμε να μειώσουμε τον αριθμό των bits κατά 69,4%. Θεωρώντας ότι υπάρχει άμεση συσχέτιση της μείωσης αυτής με την ενεργειακή απόδοση του κομματιού η προοπτική για την υλοποίηση του με χαμηλότερη κατάλληλωση είναι πλέον φανερή.

Τέλος, στην παρούσα διπλωματική συνιάστηκαν πολλές καινοτόμες ιδέες. Η τεχνολογία επικοινωνίας στα 60 GHz η οποία έχει προοπτικές για μελλοντική ανάπτυξη στην αγορά καθώς και η ιδέα των Σεναρίων Συστήματος και η παραγωγή λεπτομερών σχεδίων κβαντοποίησης για ένα στοιχείο υλικού για την αξιοποίηση της τεχνολογίας εντολών Soft-SIMD. Με αυτόν τον τρόπο η διπλωματική αυτή ανοίγει προοπτικές προς νέα συστήματα που μπορούν να συνδυάζουν την υψηλό ρυθμό μετάδοσης δεδομένων χωρίς να συμβιβάζουν την ενεργειακή τους απόδοση.
Abstract

Modern embedded systems complexity, performance and energy efficiency has been increasing steeply the last few years. An explosive growth in demand for wireless communication is observed as well and modern wireless links are expected to deliver bit rates of several gigabits while consuming even less energy.

In order to satisfy these needs new technologies emerge and novel design approaches are put into practice. Communication at 60 GHz is such a technology that is able to deliver high bit rates in short range wireless links. A major motivation to use the 60 GHz spectrum is the worldwide availability which makes exploitation economically viable. Moreover, small wavelength of only 5 mm promises high integration due to small antenna component size which is one of the main bottlenecks for reducing the dimensions.

However, increased frequency comes with many disadvantages as well. To increase the market potential of such a new technology the chip design needs to be cheap and energy-efficient. Such cost and energy constrains heavily impact the performance and the quality of both the analog and the digital components of the chip.

In the current thesis the design possibilities of a component in the digital baseband of the receiver of such a chip are explored. The component under investigation is a Fast Fourier Transform (FFT) that is used for frequency domain equalization. This part of the receiver is used to reduce the effects of multipath in a non line-of-sight communication environment and as this is a common case in wireless communication the FFT block has been identified as one of the 2 most computational intensive components of the receiver in 60 GHz. This is the main reason why we explore possibilities to further decrease the power consumption of the block while maintaining the performance and the quality of service.

To achieve this reduction the possibilities of a new design concept are explored. System Scenarios is a new design concept for embedded systems operating in dynamic environments. Wireless communication systems exhibit high dynamism during their operation on highly varying data streams, providing the System Scenarios huge
capabilities.

The essential idea behind system scenarios is the classification of
the application under investigation from a cost perspective during
design time. Then, the classification is exploited during run time re-
sulting to an overall improved implementation of the application. To
achieve this the application is broken down to run-time situations
(RTS) which are distinguishable operation modes of the application.
Then RTSs with similar costs are clustered to form system scenar-
ios. Finally for each scenario a different mapping and scheduling of
the application is generated.

In the case of the current thesis the application is the FFT and the
cost perspective is the power consumption of the component. To ex-
plot the RTS clustering in run time different quantization schemes
have been produced. These schemes have been generated based on
various properties of the data waveforms in the input of the FFT.

The thesis explores the potential of the System Scenarios as well as
the application of a quantization methodology for the FFT. Different
options of the RTS clustering and the quantization of the FFT block
are evaluated in order to come up with a more efficient implemen-
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5.1 Outlook matrix ........................................ 65
Modern consumer electronics provide an increasing amount of services to the user in a daily basis. The market demand for cheap, reliable and highly portable electronic devices pushes the boundaries of embedded system design to new unexplored areas. Mobility demands the subtraction of all cables either for data transmission or for power. To achieve this, wireless communication at higher bit rate is required without sacrificing the high energy efficiency that renders the device independent of the power grid for large time periods. The constant increase in the modern embedded system specifications has lead to the employment of innovative ideas, approaches and technologies.
1.1 Introduction to wireless communications at 60 GHz

A new technology that promises high integration and high bit rates in wireless links is communication at 60 GHz. Communication at 60 GHz has some advantages as well as some disadvantages. These are mentioned below as referred in [29]

The main advantages are:

1. The worldwide available bandwidth is huge and the allowed equivalent isotropically radiated power (EIRP) is high. Figure 1.1 shows a comparison between 60 GHz, IEEE 802.11 WLAN and ultra-wideband (UWB) systems. 60 GHz clearly offers unprecedented possibilities.

2. Moreover, the high path loss and high attenuation by walls at 60 GHz entails some advantages. First, they enable frequency reuse over small distances. Second, the multipath environment is less aggressive.

3. Finally, the possible miniaturization of the analog components – because the wavelength in free space is only 5 mm – is also a definite advantage of 60 GHz. We can for instance build antenna arrays on a very small surface area.

Opposed to this are some disadvantages:

1. The high path loss at 60 GHz means that we have to cope with a very tight link budget, even though the maximum allowed EIRP is high. Moreover, complementary metal-oxide semiconductor (CMOS) transistors offer less amplification at these high frequencies. This will tighten the link budget even further. We will explain below that we choose CMOS technology to keep the cost low.

2. Next, more stringent requirements are put on the analog components, like multi Gsamples/s analog-to-digital converters (ADCs).
Finally, non-idealities of the radio frequency (RF) front-end have a much larger impact than at lower frequencies. A suitable air interface for low cost, low power 60 GHz transceivers should thus use a modulation technique that has a high level of immunity to front end non-idealities. Moreover, the modulation technique should allow an efficient operation of the power amplifier (PA) to relax the link budget as much as possible.

The worldwide availability, high bit rates and integration possibilities render the technology of communication at 60 GHz important for future wireless applications. This is the main reason we are motivated to explore the hardware architecture of the components of its digital baseband.

But the digital part of this 60 GHz receiver has to operate at a very high data rate, which means it will also consume a large amount of energy. For a battery-driven device that is not acceptable so clever and less conventional ways to reduce that energy requirement again
are required to enable this new standard to become acceptable in overall energy efficiency. For this purpose, we are exploring a recently introduced innovative concept where we exploit the available dynamism that is inherently present in the data stream supplied to the 60 Ghz digital front end modules.

1.2 System Scenarios concept

A new design approach for embedded systems promises effective exploitation of the dynamism that a system may exhibit. Wireless communication systems typically operate in quite dynamic environments. System Scenarios [15] have a large potential to improve the efficiency of the implementation of the digital baseband of such systems.

The essential idea behind System Scenarios is the classification of the system from a cost perspective during design time and the exploitation of the classification during run time. In the present thesis we try to apply the System Scenario design methodology to improve the implementation of an FFT block located at the receiver part in the frequency domain equalization component. The basic idea is to classify the instances of the FFT (called Run Time Situations - RTS) from a cost perspective, in our case the number of bits needed to represent each signal of the FFT, and use different quantization schemes during run time to effectively reduce the power consumption of the component.

Typically, to deal with the increasing complexity of the modern embedded systems, a system is conventionally broken down in use cases. A use case is defined by the designer under a usage point of view. During run time it is defined by the user interaction with the application. In contrast, a System Scenario is characterized by a certain functionality and is defined by a resource usage point of view. At run time, the System Scenarios represent a detectable set of operation modes of a mapped application that are similar under a cost point of view on the selected platform. In figure 1.2 it is shown how the System Scenario design methodology is incorporated in the traditional embedded systems design methodology.
Σχήμα 1.2: Incorporation of the System Scenario methodology in the traditional embedded system design flow.

In this way we are able to exploit the dynamism that is observed in various parameters of a system while adding a small overhead due to the switching between the different System Scenarios during run time. However the overhead is outmatched by the gain obtained due to the dynamism. System Scenarios have been applied before, while exploiting control variables with great success, some references can be found in [28], [11], [12], [13], [14], [18] and [24]. In the current thesis however we try to apply the System Scenarios using data variables as parameters to create different System Scenarios. That is potentially more widely applicable even, but the challenges for clustering and detection are high. In order to enable the use of the detected System Scenarios at run-time, we want to exploit the dynamic variation of the quantisation requirements for the data in the data stream.
1.3 Quantization problem

When an analog signal is represented in digital format a loss in the signal precision is expected due to quantization. The problem is that a digital representation of a signal is limited by finite precision in contrast with the infinite precision of the analog counterpart. System designers deal with the trade-off between the quantization noise introduced by the lack of precision and the number of bits needed to represent a signal which increases the system cost.

Signals are representations of physical quantities such as temperature, pressure, voltage, brightness, etc. Most real-world signals are analog in nature, which means that they vary continuously in time and in amplitude. Transmitting them based on digital techniques, which are intrinsically discrete, requires quantization. Thus, quantization effects have been actively studied for more than fifty years (see survey in [22]).

The first purpose of quantization is to find a compact scheme that represents the source information efficiently and reliably [16]. New quantization effects have emerged in the early 1970’s due to the raise of digital signal processing [23]. The objective here is to understand how finite-precision signal processing differs from infinite-precision signal processing for a digital discrete-time signal processing system. It is important to discern these two topics when studying the literature.

Most of the related work assumes binary fixed-point number system (either 2’s complement or unsigned binary number) with either round-off or truncation as quantization mode [22]. They all agree in splitting the static data format analysis in two steps: range analysis and precision analysis. The range analysis provides the margin to accommodate the growth of the data (avoiding overflow), whereas the precision analysis guarantees the accuracy of the operations. Still, different approaches have been followed for range and precision analysis.

Initially, dynamic analysis methods, also called simulation-based methods, were used to approach the problem. They evaluate the data flow graph of the design using representative input signals.
Although dynamic techniques offer a full coverage of the different types of signal processing applications as they rely on real measurements of the quantization noise, they involve extremely long simulation runs which become unacceptable when targeting medium and large size systems. This is specially important in precision analysis where an iterative optimization is typically used. Also, the accuracy of the final word-lengths strongly depends on the representativity of the simulation-environment.

Later, static analysis methods, also called analytical methods, have gathered most of the community attention. They propagate statistic characteristics of the inputs through the DFG and hence no system simulations are required. Instead, static techniques depend on models of the quantization noise propagation which results in simulation runs orders of magnitude faster. However, they either cover a reduced set of applications, such as Linear Time Invariant systems, in a very accurate way or include conservative assumptions which result in over-dimensional results.

Most recent contributions consist of hybrid approaches which try to combine analytical models with a few simulations in order to provide accurate fast estimates over a wide range of signal processing applications. This last category is the most promising one, and we will extend an existing hybrid approach.

Regarding the quantization error, this is normally avoided during range analysis and controlled during precision analysis. Most of the methods ([8], [9], [27], [20] and [26]) monitor the average Signal-to-Quantization Noise Ratio (SQNR) and only a few of them ([21] and [19]) monitor the maximum absolute quantization error. Although for most applications a SQNR spec is sufficient, some others may also require an upper bound on the maximum quantization error and therefore both error metrics are of interest.

All of the above methods face difficulties either in large simulation times or heavy constrains on the properties of the system under investigation. The method proposed in [6] overcomes most of these problems and describes a more general and highly scalable approach to the quantization problem. However, it still gets in CPU time problem when large algorithmic blocks with multiply-add type
behaviour are present. That is for instance the case in the FFT. Hence, in this thesis we extend this method with a major new step to remedy that weakness. We use the modified methodology to produce different quantization schemes for each System Scenario of the FFT. These can then be exploited at run-time, whenever a new system scenario instantiation is detected. But that still requires a suitable processor platform where the dynamically varying word-length requirements create highly varying energy results. This will be enabled by exploiting a so-called soft-SIMD platform (see below).

1.3.1 Single Instruction Multiple Data

The Single Instruction Multiple Data (SIMD) (Figure 1.3) instructions are used to increase the performance of applications since they execute one instruction on different data at the same time. The SIMD exploits the data parallelism that is contained in applications, for e.g. in multimedia. It can be performed using hardware or software.

![Figure 1.3: Application of SIMD.](image)

The Hardware SIMD (Hard-SIMD) (Figure 1.4) is currently used by energy efficient high performance processors, which provide special hardware in their data path to support combinations of sub-words of the same length, e.g. 1x64bits, 2x32bits, 4x16 bits or 8x8 bits. The limited number of different sub-words sets the ceiling of the data to the next available power-of-2 hardware sub-word, which leads to unused bits and therefore loss in efficiency. Moreover, different Hard-SIMD implementations are incompatible with each other, due to the fact that each implementation provides a
number of SIMD and a set of pack and unpack instructions based on the target architecture, leading to low portability of the application.

![Diagram of Hardware SIMD with 16 bits sub-words.](image)

Σχήμα 1.4: Hardware SIMD with 16 bits sub-words.

The Software SIMD (Soft-SIMD) (Figure 1.5) is independent of the target architecture providing portability of the application. The Soft-SIMD does not require specific hardware support and as a result of this, additional instructions must be inserted in order to guarantee the functional correctness. Hence, the Soft-SIMD speed up in performance is lower than for the Hard-SIMD, but due to the flexibility of the sub-words it can explore the word-length information by making more efficient combinations. It is this flexibility that we try to exploit by producing more efficient quantization schemes for each hardware component.

![Diagram of Software SIMD with different sub-words.](image)

Σχήμα 1.5: Software SIMD with different sub-words.

The Soft-SIMD can improve the performance, the energy efficiency and the flexibility. By applying SIMD, Soft or Hard, the increase in parallelism leads to reduction in the number of operations performed on the data and of accesses to the instruction memory. As fewer operations have to be scheduled, performance can be improved. For Soft-SIMD, care must be taken in order not to lose the obtained gain due to the insertion of the extra operations for correction, such as packing and masking operations. Soft-SIMD is able of packing different sub-words leading to more efficient paralleliza-
tion and also enables the usage of SIMD in applications that cannot benefit from Hard-SIMD, e.g. the applications where the minimum sub-word is larger than the supported sub-words in hardware.

The Feenecs template developed at IMEC presented in [7] supports the Soft-SIMD approach and motivates us to further explore the implementation possibilities of the FFT block by using various quantization schemes. As the clustering of the operations leads to fewer operations, we assume that the reduction in the number of bits needed to represent the FFT internal signals is directly linked to the power consumption of the block. Thus based on the combination of the System Scenarios concept and the different quantization schemes, we try to end up with a more power efficient implementation of the overall block under dynamic conditions.

1.4 Thesis contributions and structure overview

In the present thesis we explore the hardware architecture possibilities of the FFT located at the receiver side of a 60 GHz transceiver. The FFT is part of the frequency domain equalization component used to reduce the effects of multipath. Using system scenarios we try to end up with a more adaptable and therefore more energy-efficient FFT implementation. The application of the System Scenarios using data as parameter is a novel approach and in this work we test its feasibility. To achieve that we also need to produce efficient quantization schemes of the FFT in acceptable time intervals. Current quantization methods do not yet provide such a possibility. Thus based on the extension of an existing methodology we propose a complete methodology that can produce quantization schemes of large hardware components like the FFT.

The structure of the thesis is as follows:

- In chapter 2 an overview of the 60 GHz technology is given as well as some details of the Matlab model that was used for simulations.
- In chapter 3 the problem of quantization of hardware signals
is presented. Moreover the baseline quantization methodology is described as well as the modification done to make it usable in our case.

• In chapter 4 the concept of System Scenarios is described in detail as well as the set up of our experiments and their results.

• Finally, in chapter 5 the conclusions and the prospective future work of the thesis are presented.
In modern wireless communication the demand for high bit rates with low power consumption is steeply increasing. In order to satisfy the needs of modern wireless systems new technologies emerge that are able to deliver these increased rates. Communication at 60 GHz is such a technology that is able to deliver high bit rates in short range wireless links.

2.1 Motivation of using the 60 GHz spectrum

A major motivation to use the 60 GHz spectrum is the worldwide availability which makes exploitation economically viable. While unlicensed spectrum around 2.5 GHz and 5 GHz is also available internationally, the amount of available 60 GHz bandwidth is an order of magnitude above that available at 2.5 GHz and 5 GHz. This is shown in Figure 2.1 as presented in [29].

Below a brief list is presented ([30]) with the various regulations
that exist worldwide.

- **America** In 2001, the United States Federal Communication Commissions (FCC) allocated 7 GHz in the 54–66 GHz band for unlicensed use.

- **Japan** In year 2000, the Ministry of Public Management, Home Affairs, Posts, and Telecommunications (MPHPT) of Japan issued 60 GHz radio regulations for unlicensed utilization in the 59–66 GHz band. The 54.25-59 GHz band is however allocated for licensed use.

- **Australia** Following the release of regulations in Japan and North America, the Australian Communications and Media Authority (ACMA) has taken a similar step to regulate 60GHz band. However, only 3.5GHz bandwidth is allocated for unlicensed use, that is, from 59.4–62.9GHz.

- **Europe** The European Telecommunications Standards Institute (ETSI) and European Conference of Postal and Telecommunications Administrations (CEPT) have been working closely to establish a legal framework for the deployment of unlicensed 60 GHz devices. In general, 59–66 GHz band has been allocated for mobile services without specific decision on the regulations.
Apart from the large availability worldwide another motivating feature is the small wavelength of only 5 mm that promises high integration due to small antenna component size. The latter is one of the main bottlenecks for reducing the dimensions.

2.1.1 Technical Challenges

Despite many advantages offered and high potentials applications envisaged in 60 GHz, a number of technical challenges and open issues remain present that must be solved prior to the successful deployment of this technology. To increase the market potential of such a new technology the chip design needs to be cheap and energy-efficient. Such cost and energy constrains heavily impact the performance and the quality of both the analog and the digital components of the chip.

As far as the integrated digital circuits are concerned the significantly increased bit rate demands increased computational ability of the receiver side while the power consumption must remain to low level to maintain the mobility of the wireless devices. This introduces new design challenges for the implementation of the hardware components.

2.1.2 Future applications

Although the need for wireless broadband connections is growing the usage of 60 GHz spectrum for outdoor applications is limited due to its low range and the high cost of components needed to achieve line-of-sight communication of up to the range of a couple of kilometres.

The prospect for the usage of the 60 GHz spectrum for indoor gigabit communication is very likely. For commercial usage the 60 GHz can be used for Wireless Local Area Networks (WLANs) where the technology can deliver gigabit connections that the current wireless technologies cannot deliver. The range is limited in a single room though, something that suggests hybrid solutions that will combine 60 GHz and standard WiFi connections.
Another possible application is the usage for Wireless Personal Networks such as Bluetooth technology. The prospective use of the technology is the replacement of USB connections, IEEE 1394 Firewire, gigabit ethernet as well as multimedia delivery. These connections are most likely to be replaced by 60 GHz components in the future as the ultrawideband (UWB) spectrum (3 - 10 GHz) that is able to deliver such wireless links suffers from the fact that the spectrum is not worldwide available and that its bandwidth may not be able to deliver demanding future applications.

Finally, high definition video transmission even in raw format can be transmitted using the 60 GHz replacing any cables around televisions and projectors ([1],[3],[4]). This is the most likely commercial use of the 60 GHz spectrum and this is the reason the current thesis uses raw and encoded video transmission as reference in most simulations.

### 2.2 Channel modes and channel models

In this work we carry out our experiments using a near ideal channel. In all experiments the single carrier transmission is chosen as well as minimum noise. Such condition can and will typically occur in line-of-sight wireless links of very short distance (up to a few meter). In the next two sections we explore various realistic channel modes and channel models. Using these modes the experiments can be carried out and based on that it should be possible (as future work) to generalize the findings of this work.

#### 2.2.1 IEEE 802.15.3c standard specifications

In this section the IEEE 802.15.3c ([5]) standard concerning the single carrier transmission is explored in order to find modes that can be encountered frequently and that may have aspects that can be exploited in implementation level but not in functionality level due to standards restrictions. The basic modes of the standard are analysed and the mandatory features are distinguished.
Single Carrier PHY

The systems of 802.15.3c standard are categorized in three classes as seen in table 2.1. Each class uses different modulation and coding schemes (MCS). Generally Single Carrier PHY support $\pi/2$ BPSK / $\pi/2$ QPSK / $\pi/2$ 8PSK / $\pi/2$ 16QAM modulation and line-of-sight operation as well as non line-of-sight.

<table>
<thead>
<tr>
<th>Class</th>
<th>Categorization</th>
</tr>
</thead>
<tbody>
<tr>
<td>Class 1</td>
<td>Data rates &lt; 1.5 Gb/s</td>
</tr>
<tr>
<td>Class 2</td>
<td>1.5 Gb/s &lt; Data rates &lt; 3 Gb/s</td>
</tr>
<tr>
<td>Class 3</td>
<td>Data rates &gt; 3 Gb/s</td>
</tr>
</tbody>
</table>

Πίνακας 2.1: Modulation - coding schemes categorization for the single carrier PHY

Modulation

The mandatory modulation and coding schemes defined by the standard are the common mode signalling (CMS) that is used for recognition between devices. It is used between two devices that start to communicate that do not know each other’s capabilities. Through CMS the best possible combination of parameters that is supported in both devices is found and is used for optimal communication. In order for CMS to be in any device that obeys the protocol it means that it is designed for compatibility and not for performance. So at the functionality level not all possible optimisations will have been exploited, which leaves some room for further exploitation at the implementation level. But the problem is that the mode in general is not used for a large period of time so it is not frequent enough to be exploited in the system scenario paradigm (see section xxx). It always used for recognition which last a tiny period of time and although it could be used for data transmission it is more probable that after the recognition more efficient schemes will be used.

Another mandatory MCS is the PHY Rate (MPR). In figure 2.2 it is shown the MCS dependent parameters that gives a good perspective of what modes can be encountered. Also two optional modulation
modes OOK and DAMI exit which use simplified constellations for mapping.

As seen in the figure, in class 1 MCS the modulation used is $\pi/2$ BPSK. Also in the same class we encounter CMS and MPR. We can see that CMS has the lowest data rate and it is the only one using a spreading factor of 64. The other mandatory MCS is MPR and it seems to have a decent data rate. It uses $\pi/2$ NPSK modulation as well and the spreading factor is 1.

**Fig. 2.2:** MCS dependent parameters

As seen in the figure, in class 1 MCS the modulation used is $\pi/2$ BPSK. Also in the same class we encounter CMS and MPR. We can see that CMS has the lowest data rate and it is the only one using a spreading factor of 64. The other mandatory MCS is MPR and it seems to have a decent data rate. It uses $\pi/2$ NPSK modulation as well and the spreading factor is 1.

**Coding**

In figure 2.2 we can also notice that the MCS mode uses Reed-Solomon (255,239) coding which is mandatory as well. But for high performance usage at least Class 2 should be used. The modulation here is $\pi/2$ QPSK and the spreading factor is always 1. Apart from a mode where Reed-Solomon is used all other cases use LDPC coding. For highest performance class 3 modes LDPC coding is required. However, LDPC is optional.
Spreading

As far as spreading is concerned generally the spreading factor is set to 1 except for some class 1 modes where spreading factor of 64 is used (using Golay sequences) as well as factors of 2 and 4. In the case of OOK mode with a spreading factor of 2 a simple bit repetition in which each bit shall be repeated twice is used.

Timing

In the above figure we can see the parameter pPHYChannelSwitchTime which is the maximum time that may elapse for a channel switch to take place (100ns). The pPHYSIFS\(_{\text{Time}}\) is the minimum time between successive transmissions. A maximum frame size is 8388608 octets and the minimum fragment size is 512 octets.

Selection

Considering all the above and taking into account how a real application may look like among all 13 different MCS modes we have selected MCS 3 and MCS 11.

Motivation

The selection criteria for our choice are mostly how frequent an application may use a mode and for how much time. Moreover we have taken into account that a MCS mode should also exploit the
benefits of the 60GHz context. This may not be as obvious but if the high rate produced by the 60GHz is not exploited by the application then the usage of another standard for wireless communication is a better candidate for usage in the application. So high rated modes are most favourable. Finally, as already mentioned, mandatory features that will be implemented in all future devices are in favour as communication through them is more probable in an environment with various devices.

The MCS modes that have been selected are:

- MCS 3 (BPSK Modulation, Rsym = 1650Msym/sec, Reed-Solomon coding)
  - This is a mandatory single-carrier mode (MPR - mandatory PHY rate). Therefore, all SC devices have to support it. High-end devices are designed for far tighter specifications so we can probably exploit this "margin" at the implementation level.
  - The high rate is representative for 60GHz. The usage of 60GHz communication is justified.
  - The standard does not indicate in which scenarios it has to be used. Probably it is a sort of a backup mode, still to be investigated.

- MCS 11 (QPSK Modulation, Rsym = 3300Msym/sec, Reed-Solomon coding)
  - This is the highest rate that can be supported with QPSK. QPSK is a good case study because it will definitely be adopted by industry. Moreover, it is a mathematically convenient case study because I and Q channels can be treated independently. Finally, we can make QPSK captures in the lab, which could lead to a very strong research paper (if we can apply our concepts to this real-world data).
  - The high rate can only be supported with 60GHz, so it is a good case for 60GHz technology.

Apart from the reasons that we selected the above modes it is good to mention reasons why we did not select other modes. The CMS
mode which will be used frequently by all devices to begin communication. But as already mentioned, it is not selected because the rate is very low for any data communication and the usage although frequent would not last long as after the connection is established the devices will immediately switch to more effective MCS.

The class 3 MCS are rejected mostly because of their modulation. The other modes of class 2 are rejected due to lower rate and due to a preference to Reed-Solomon coding.

2.2.2 IEEE channel models

IEEE has modelled some reference channels to be used in Matlab simulations. As it is not possible to generate a single generic channel model these models are based mostly on experiments and some rough approximations. In the committee report the channels in Table 2.2 are mentioned.

From these models the ones that are worth exploring are considered models CM1 and CM2 which are for residential use as well as CM3 and CM4 which are for office use. Both line-of-sight and non line-of-sight in these cases are considered to be really frequent in future commercial applications thus further exploration is motivated.

2.3 Matlab transceiver model

In IMEC Leuven a Matlab transceiver model has been developed to simulate a single wireless transmission through a 60 GHz channel. The model is able to send a series of frames of data. Many components of the digital baseband are parametrizable such the digital filter as well as the modulation scheme, the number of frames transmitted, the input data, the channel model and the noise injections to the signal.

The model output is the bit error rate of the data received by the receiver. In this way when one if the parts in the digital baseband is quantized we can get the degradation caused due to the quantiza-
<table>
<thead>
<tr>
<th>Channel Model</th>
<th>Scenario</th>
<th>Environment</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CM1</td>
<td>LOS</td>
<td>Residential</td>
<td>Typical home with multiple rooms and furnished with furniture, TV sets lounges, etc. The size is comparable to the small office room. The walls/floor are made of concrete or wood covered by wallpaper/carpet. There are also windows and wooden door in different rooms within the residential environment.</td>
</tr>
<tr>
<td>CM2</td>
<td>NLOS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CM3</td>
<td>LOS</td>
<td>Office</td>
<td>Typical office setup furnished with multiple chairs, desks, computers and work stations. Bookshelves, cupboards and whiteboards are also interspersed within the environment. The walls are made by metal or concrete covered by plasterboard or carpet with windows and door on at least one side of the office. Cubical, laboratory, open and closed office can be treated as a generic office. Typically these offices are linked by long corridors.</td>
</tr>
<tr>
<td>CM4</td>
<td>NLOS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CM5</td>
<td>LOS</td>
<td>Library</td>
<td>Typical small size library with multiple desks, chairs and metal bookshelves. Bookshelves are filled with books, magazines, etc. Some tables and chairs were interspersed between the bookshelves. At least one side of room has windows and/or door. The walls are made of concrete.</td>
</tr>
<tr>
<td>CM6</td>
<td>NLOS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CM7</td>
<td>LOS</td>
<td>Desktop</td>
<td>Typical office desktop and computer clutter. Partitioning surrounded this environment.</td>
</tr>
<tr>
<td>CM8</td>
<td>NLOS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CM9</td>
<td>LOS</td>
<td>Kiosk</td>
<td>Typical Kiosk server with human body holding a portable device. The portable device is pointed to the kiosk server.</td>
</tr>
</tbody>
</table>

Πίνακας 2.2: Channel models that can be generated by the channel generation function provided by IEEE
2.3.1 Input data

To carry out the experiments various input data have been used. These are the following:

- **Random data** Additive white Gaussian noise generated by Matlab has been used. Using this noise there is no data correlation among the input data.

- **Raw video** Raw video input has been used. In this case strong correlations among the transmitted data are observed. The raw video format was YUV and is presented in the paragraph below.

- **Encoded video** Encoded video input has been used as well. In this case most data correlations from the raw video do not exist but we can assume that the coding is not perfect so that minor correlations among the data can be observed. The main reason why the coders are in practice not removing all data correlations, is that for the general video case, the algorithms to realize that would be way too costly to implement. As a result, quite some correlations can be left in the incoming data stream.

2.3.2 YUV raw video and SVC Encoding

**YUV raw video format**

YUV is a color space typically used as part of a color image pipeline. It encodes a color image or video taking human perception into account, allowing reduced bandwidth for chrominance components, thereby typically enabling transmission errors or compression artifacts to be more efficiently masked by the human perception than using a "direct" RGB-representation.
The YUV model defines a color space in terms of one luma (Y) and two chrominance (UV) components. The YUV format uses 6 bytes to represent 4 pixels. Each pixel gets a Y value and every four pixels share a U and a V value. The means that to represent four pixels 48 bits are needed, an average of 12 bits per pixel. In figure 2.4 the position of the data on a frame is shown.

![Single Frame YUV420](image)

**Position in byte stream:**

**Σχήμα 2.4: A single YUV frame**

The video used is a 1280x720 resolution video. That means that each video frame consists of 921,600 pixels. As a single video frame consists of 11,059,200 bits in order to send a video frame in various modulations we need many frames. This is shown in table 2.3.

<table>
<thead>
<tr>
<th>BPSK</th>
<th>QPSK</th>
<th>8PSK</th>
<th>16QAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bits per frame</td>
<td>28672</td>
<td>57344</td>
<td>86016</td>
</tr>
<tr>
<td>Frames per video frame</td>
<td>386</td>
<td>193</td>
<td>129</td>
</tr>
</tbody>
</table>

**Πίνακας 2.3: Bits and frames needed for various modulations**

**Motivation for the SVC coding**

SVC can be considered an encoder that will be used commercially in telecommunications for the next years as it has great features concerning complexity and performance. An encoder with even better performance will increase the complexity in an exponential way making it extremely difficult to efficiently implement it in an embedded system. And the complexity added in SVC compared to the
previous encoder generation (MPEG-4) is reasonable regarding the performance gain.

The above conclusion is based on [10]. We can see in figure 2.5 that as the layers increase and we have a more efficient encoder the complexity increase exponentially. Considering that layer one in the figure is actually MPEG-4 it is safe to say that future encoders' complexity will be restricted. So SVC is a good encoder for commercial use as it combines good characteristics both on complexity and on efficiency.

![Figure 2.5: Impact of inter-layer prediction on the SVC decoder computational complexity](image)

**Figure 2.5: Impact of inter-layer prediction on the SVC decoder computational complexity**

### 2.4 Digital Baseband

The two most computational intensive components of the digital baseband of the receiver is the digital filter and the Fast Fourier Transform. The whole digital baseband is summed up in table 2.4. As shown in the table the complexity of the digital filter and the frequency domain equalization is significantly higher than any other block of the digital baseband.

The frequency domain equalization [2] is used to reduce the effects of multipath that appear in non line-of-sight wireless links. The preference for frequency domain equalization (FDE) instead of time domain equalization is because of the reduced complexity of the former and the fact that the FDE performance with single-carrier
<table>
<thead>
<tr>
<th></th>
<th>MAdd / sec</th>
<th>MMulti / sec</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Digital Filter</strong></td>
<td>83</td>
<td>86</td>
</tr>
<tr>
<td>IQ compensation</td>
<td>10</td>
<td>6</td>
</tr>
<tr>
<td>CFO compensation</td>
<td>6</td>
<td>8</td>
</tr>
<tr>
<td><strong>FFT + Eq + IFFT</strong></td>
<td>117.5</td>
<td>117.5</td>
</tr>
<tr>
<td>Tracking + TS Removal</td>
<td>7</td>
<td>6</td>
</tr>
<tr>
<td>Tx IQ compensation</td>
<td>12</td>
<td>10</td>
</tr>
<tr>
<td>Synchronization</td>
<td>444</td>
<td>7</td>
</tr>
<tr>
<td>Channel estimation</td>
<td>480</td>
<td>38</td>
</tr>
</tbody>
</table>

Πίνακας 2.4: Relative complexity comparison of the PHY 60 GHz layer blocks.

(SC) is similar to that of orthogonal frequency-division multiplexing (OFDM). Moreover the use of the FDE makes the SC design compatible with that of the OFDM leading to more integrated implementations.
3.1 Data representation

In this section the various data representations used in modern embedded systems are presented. A distinction between signals and coefficients is made as they have different properties and use different representation formats.

3.1.1 Signals and fixed-point arithmetic

Data representation in the implementation of an embedded system is very crucial. Many different number representation systems have been used but the most common by far are the floating point and the fixed-point representations. The first one gives the opportunity to the designers to ignore any problem that occurs due to finite precision because it provides very high dynamic range and normalization after each operation abstracting the radix-point. However this
leads to large word-lengths and complex operators that increase the implementation cost. In [17] a difference of 10x increased energy consumption between a floating point implementation and a fixed-point alternative is stated.

On the other hand fixed-point requires radix-point alignment during the design time analysis, and it reduces the dynamic range. Still, this is preferable when the energy consumption and system cost are crucial objectives of the system. Figure 3.1 shows a typical fixed-point representation consisting of an integer part and a decimal part. Typically an extra bit in the MSB part is used as sign bit but it can be omitted in case of unsigned data. In this arithmetic family the decimal point indicates where the power of '0' is in the number representation.

![Figure 3.1: Fixed Point Representation](image)

The numbers in each box represent the power in which each bit is raised. As we use 2-complement arithmetic the most significant bit is a negative number and all the other positive (but there is no extra sign bit). So the mathematical formula is: \( (x(n) \) is the \( n_{th} \) bit of the binary number)

\[
X = -2^N x(N) + \sum_{n=0}^{n=N-1} 2^n x(n) + \sum_{m=1}^{m=M} 2^{-m} x(m)
\]  

(3.1)

For example the fixed-point number 110.101\(_b\) is calculated as: integer part: \(-1 \cdot 2^2 + 1 \cdot 2^1 + 0 \cdot 2^0\) and decimal part: \(1 \cdot 2^{-1} + 0 \cdot 2^{-2} + 1 \cdot 2^{-3}\) that equal to \(-2_{10} + 0.625_{10} = -1.375_{10}\).
**Fixed-point noise introduction**

When the fixed-point arithmetic is used two different kind of errors can be introduced to the system due to the number representation. In the case the number is larger than the maximum that can be represented an overflow error occurs. In order to avoid such errors the integer part of the representation must be large enough. This can be calculated at design time with a data dynamic range analysis. In the current work, based on a simplified analysis and bounding we have decided that the integer part is large enough and no overflow errors occur.

On the other hand, also a quantization error at the LSB side is introduced in the system due to the finite precision used to represent a continuous signal. This error is limited by the position of the LSB with respect to the radix-point. The further it is to the right the smaller the quantization step and the smaller the quantization error. The possibility of bounding the quantization error enables to introduce approximate signal processing while still providing a guarantee of minimum quality of service. Notice that for a continuous-amplitude input signal, this quantization error is unavoidable, as opposed to the previous overflow error. Accordingly, the final signal’s word-length, $\lambda$, is confined by the MSB and LSB positions.

Before starting the quantization procedure, the maximum degradation that can be caused to the system due to quantization noise is defined and it is called error budget or noise budget. This is typically achieved by the functionality team and in the case of the 60 GHz transceiver it has been expressed as Bit Error Rate (BER) degradation in the output of the receiver. Using this degradation as a constraint we try to find the optimal distribution of the error budget among the system signals.

As it becomes clear when using the fixed-point format, two important signal attributes should be taken into account. These are used to determine the appropriate number of bits for the representation of both the integer and the decimal part of a signal. Briefly these are:
**Dynamic Range**  The range of the values of the signal. It is used to calculate the number of bits needed for the integer part of the representation.

**Precision**  The accuracy of the representation of the signal. It is increased by increasing the bits used to represent the decimal part of the signal.

In the following paragraphs these attributes are explained in greater detail.

**Dynamic Range**

Like all other representation formats, the fixed-point has a finite dynamic range. Dynamic range is the range of values that the format can represent. In the case of the fixed-point format the needed dynamic range determines the integer part. To find the dynamic range of a signal (the range of the values that are required to be represented as in Figure 3.2) first it is required to sample as many values as possible that the signal gets. Then among these values the absolute maximum value is the value that defines that signal's dynamic range. The algorithm 1 is used to find the dynamic range of a signal.

![Σχήμα 3.2: Dynamic Range of a signal](image)

The dynamic range of a fixed point representation is defined by its maximum and the minimum value that it can represent. The minimum value can be calculated by equation 3.2 and the maximum iteratively like in algorithm 2. In both cases INT is the number of
Algorithm 1 Dynamic range of a signal

procedure Dynamic Range(signal)
    max ← 0;
    for ii = 1 : length(signal) do
        if max ≤ |signal(ii)| then
            max ← |signal(ii)|;
        end if
    end for
    dynamic_range ← max;
end procedure

integer bits and DEC is the number of decimal bits. To effectively increase the dynamic range of the representation additional bits in the integer part should be added. That is why in the quantization procedure the integer part of a signal is determined by the dynamic range of the signal's values.

\[
minimum\_value = -2^{(INT-1)}
\] (3.2)

Algorithm 2 Maximum value of a FXP representation

procedure FXP max value(INT,DEC)
    max ← 0;
    for ii = 0 : INT-2 do
        max ← max + 2^ii;
    end for
    for ii = 1 : DEC do
        max ← max + 2^{-ii};
    end for
end procedure

Precision

The precision of an arithmetic representation indicates the distance between two consecutive numbers (Figure 3.3. If the distance is
large, all the values between the two numbers are quantized to either side of the interval (based on the quantization policy) and an error is introduced proportional to the distance that a value has been shifted. This distance can be decreased by increasing the bits in the decimal part of the representation. As more bits are added the shifting distance diminishes and the less the error introduced. The trade-off between the number of decimal bits and the quantization error is the one explored during the quantization analysis and it is the reason why the quantization method should be introduced.

Σχήμα 3.3: Precision of the representation of a signal in a quantized format

### 3.1.2 Coefficients and canonical signed digit format

Although it is common to represent the signals using FXP format the constants are usually represented using CSD (Canonic Signed Digit) format. Obviously, constants with minimum non-zero bits are preferred, as they require less operations leading to cheaper implementations. Thus, constants are coded in a CSD form. CSD representation reduces on average 33% the non-zero bits compared to a two’s complement representation [25].

The representation uses a sequence of one or more of the symbols, -1, 0, +1 (alternatively -, 0 or +) with each position possibly representing the addition or subtraction of a power of 2. For instance
23 is represented as +0-00-, which expands to +2^5 − 2^3 − 2^0 or 32 − 8 − 1 = 23.

In the case of the FFT quantization the constants that needed CSD format are its coefficients. Thus the budget is allocated among signals and coefficients and they are quantized separately.

**Coefficient optimization in CSD format**

To optimize the CSD representation of each coefficient the generate CSD options (gen_CSD_options) function was used. This function gets as input the floating point value of the coefficient as well as the number of bits that are used for its representation and it returns a Pareto curve with all the possible representations. For example when the number 0.45 with bit range from 1 to 24 bits the output is depicted in Figure 3.4.

![Figure 3.4: Pareto curve of the representation of 0.45 value using 1 to 24 bits. In the Y axis is the number of non-zero bits and in the X axis is the quantization error introduced to the constant value.](image)

The function returns the various values that the constant gets using different number of non-zero bits. Using these values we travel across the Pareto curve from maximum degradation to the exact value and stop to the point that satisfies the noise constraint of the coefficient. In this way we can find the minimum number of non-zero bits that we need to represent the coefficient.
3.2 Quantization procedure for signals

The quantization problem consists in finding the fixed-point representation of the FFT block which minimizes a particular implementation cost - in our case total energy consumption - while still providing the required functional performance. However it is not possible to exhaustively search all the quantization options for the FFT block and find an optimal one. For this reason the following systematic methodology is used which is presented in [6]. Using this methodology the search area is heavily pruned and still a near optimal solution is found. In simple systems the solution typically turns out to be fully optimal.

3.2.1 Quantization Standard Method

To apply the method we need to use the following hierarchical approach to the system as shown in Figure 3.5. To partition each level the actions needed on the right need to be done.

- **System Level** Starting from system level an error budget is defined - typically by the functionality team. This is the maximum degradation that can be caused to the system output due to quantization noise. In the case of the 60 GHz the budget was 1.2 dB of BER degradation at the output of the receiver. Then the system is partitioned in functional partitions. In the case of the 60 GHz these functional partitions are the digital filter, the FFT block (including the inverse FFT of the FDE) the offset comparison, the demapping, the MIMO and the FEC decoding as shown in Figure 3.6.

Once the partitioning is done the error budget must be distributed among the functional partitions. This can be done either by distributing the budget evenly as in the case of this thesis or by using a certain metric. In the case a metric is used various properties of the partitions are taken into account. The metric proposed is the combination of the component’s hardware cost and its influence to the system output. The first is calculated by the hardware team and takes into account the
Σχήμα 3.5: System hierarchy used to partition the system in smaller components that are easier to be dealt with. On the right the actions needed to proceed to the next level are described.

Σχήμα 3.6: Partitioning the 60 GHz receiver in functional partitions. The budget distribution is shown when a metric is it is even or a metric is used.

complexity and the frequency of usage of each component. To calculate the influence of each component to the system’s output each component is degraded by the same way in all partitions (e.g. reducing all signals by one bit) and the degradation caused to the system output indicates the partition’s sensitivity - the higher the degradation the more sensitive the partition is. By using different hardware costs we can get different sen-
sitivity measurements and end up with Pareto curves of cost and sensitivity for each one of the partitions. Based on the design specifications choosing a point on the curve generates a different weight and a different distribution of the error budget in functional partitions level.

To isolate the FFT from the 60 GHz model and make the simulations easier and faster the budget allocated to the FFT has been translated to Signal to Noise Ratio (SNR) at the FFT output. This has been achieved by gradually adding white noise to the FFT output until the system's output reaches maximum allowed degradation. The addition of white noise is motivated because quantization noise typically resembles white noise. It has been found that the SNR at the output of the FFT should be at least 23dB.

- **Functional Partition Level** The FFT block is already a functional partition itself. This partition needs to be broken into smooth clusters. A smooth cluster is a cluster that does not contain any unsmooth operators. An unsmooth operator is a decision making operator like a threshold, saturation prior to a mapping to symbol operation. However the FFT block contains only additions and multiplications which are smooth operators and consists of a huge smooth cluster as it is. Normally the method distributes the error budget among the different smooth clusters using the same logic as described in functional partition level budget distribution but as the smooth cluster and the functional partition coincide in the case of the FFT block the budget needs no further distribution at this point.

- **Smooth Cluster Level** Once the smooth clusters have been detected the signals inside each clusters are grouped in correlation groups. The correlation of two signals $A$ and $B$ is determined by the correlation factor $\gamma_{AB}$. This factor indicates whether the noise injected by signal A influences the quantization of signal B and it is calculated by equation 3.3

$$
\gamma_{AB} = 1 - \frac{BER_A + BER_B}{BER_{AB}}
$$

(3.3)
where $BER_A / BER_B$ corresponds to the BER performance of the system evaluated in floating point precision but for the signal $A / B$ which is configured to the fixed-point position which maximally degrades BER performance without violating system degradation constraint (lower bound in cost).

- If $\gamma_{AB} = 0$, the errors injected by each signal are not correlated, thus signals A and B are independent.
- If $|\gamma_{AB}| \sim 0$, the errors injected by each signal are weakly correlated, thus the two signals can be solved separately in an ordered way giving priority to the most costly signals.
- If $|\gamma_{AB}| \gg 0$, the errors injected by each signal are strongly correlated, thus the two signals have to be solved together in order to avoid large iterations in the convergency process.

After the correlation all signals within a cluster is characterized, the most highly correlated signals are grouped together in correlation groups. Once again the error budget is distributed across groups according to a metric as already mentioned.

• **Correlation Group Level** Once the groups are formed each group is solved. Prior to solving a group the signals inside a group have to be ordered and quantized individually one by one. The metric used to order the signals is sensitivity. Sensitivity of a signal express the influence a signal has on the output of the cluster. The more sensitive signals are prioritized and are solved first.

The above hierarchical approach prunes the search space and avoids the processing time explosion that happens in the case of an exhaustive search. However, in the case of the FFT block using this approach is already time consuming. As already mentioned the FFT is a large smooth cluster having many signals. A 512 FFT consists of $512 \cdot 2 = 1024$ signals in each stage. It has $\log_2(N) + 1 = 10$ stages which means a total of 10240 signals (without taking into account
the coefficients and the internal signals of the butterflies. Considering that a quantized FFT calculation takes 0.626 seconds to calculate the correlation of a single signal to all the others signals of the FFT takes 1.8 hours. This makes it clear that even for calculating the correlations among the signals is not feasible in the context of the current thesis and for this reason some changes have been made to the above procedure to reduce the quantization time by decreasing the quality of the quantization. As the current thesis does not aim to an optimal quantization of the FFT, this is acceptable and the modifications made are described in the following section.

### 3.2.2 Modifications to the standard method

In order to reduce the execution time of the FFT quantization script some properties of the FFT have been investigated and exploited. The algorithm is implementing using as a basic block the butterfly. The butterfly gets as input two complex numbers and a coefficient and has at its output two complex numbers, as shown in Figure 3.7. The butterfly can be considered as a 2x2 FFT transform. As is shown in Figure 3.8 by replicating a butterfly and adding a new stage we can create the 4x4 FFT. If the process is repeated the 8x8 FFT can be produced and the process can be repeated until we get the 512x512 FFT we need (or the NxN FFT to generalize).

The basic assumption that is done before proceeding to the simplification of the FFT quantization process of the FFT block is that the input data in the first stage of the FFT is uniform. This assumption is pretty much valid as shown in Figure 3.9. The inputs are uniform apart from some spikes at the sides of the FFT. These spikes are not taken into account in present work but can be investigated in future work. The same assumption is made for all the intermediate stages of the FFT. Again through simulation using the 60 GHz transceiver model this assumption was confirmed.

To trim the search space even more the signals that belong to the same stage and in butterflies with the same coefficients are quantized in the same way. This was done because the sensitivity as well as the dynamic range and precision of the data in these butterflies
The basic FFT butterfly. Apart from being the building block of the transform it can also be considered as a 2x2 FFT as well.

By repeating the 2x2 FFT and adding an extra stage the 4x4 FFT can be produced.

have very close values that in a detailed analysis may lead to minor quantization differences but in a rough analysis like the one that we try to achieve can be safely ignored. The signals that are quantized the same way are named repetitions. The quantization procedure has been changed as well. The modified procedure is presented in Figure 3.10

As the correlation analysis was not feasible it was skipped. However it can still be done among repetitions if needed. Instead of grouping in correlation groups the repetitions are identified throughout the FFT. Instead of having 10240 signals (full fine-grain quantization) the repetitions treat those signals as if they were just 1023. As no explicit groups are present, the ordering of the signals as well as the budget distribution has been modified. Instead of ordering the signals based on their significance the FFT has been quantized from the input to the output. The reason for doing this is that the signals that are being quantized are not affected by any unquantized
Σχήμα 3.9: Histogram of the FFT input values. The values are uniform apart from some spikes in the sides of the FFT

In order to make this quantization method feasible the budget should be preallocated throughout the repetitions. To distribute the budget, a weight has been calculated for each one of the repetitions and then normalized to show percentage of the total FFT cluster that corresponds to each repetition. To calculate the weight the formula in 3.4 as used. Each weight is explained in detail below.

\[
W_{stg\_coe} = W_{rep} \times W_{sens} \times W_{distr}
\] (3.4)
Σχήμα 3.10: Modified quantization procedure used to further reduce the solution search space and make the FFT quantization feasible.

- $W_{stg,coef}$ stands for stage coefficient. It is the final non-normalized weight that allocates the budget to each repetition. We should note that a repetition in the FFT is fully defined by its stage and its coefficient.
• $W_{rep}$ It is a weight that represents the hardware cost of the current batch of butterflies. It is a normalized weight of how frequently a butterfly appears throughout the FFT. The higher the frequency the higher the hardware cost because it means that in each FFT iteration the butterfly will be calculated more than once. For example, in the case of the 4x4 FFT in Figure 3.11, the total number of butterflies is 12. The butterflies in the 1st stage which consist of a single repetition repeat 4 times throughout the FFT. So their $W_{rep} = 4/12 = 0.33$. On the other hand, the butterflies in the final stage repeat only once so their $W_{rep} = 1/12 = 0.083$. This happens because when the FFT will be calculated the first butterfly will be calculated 4 times adding more to the hardware cost than the final butterflies.

• $W_{sens}$ To take into account the influence of each repetition to the output of the FFT the $W_{sens}$ is taken into account. The sensitivity of each repetition is calculated. To do that, each repetition is first degraded in the same way and the noise caused to the system output is measured. As the signal values vary a lot throughout the FFT for this reason instead of adding an offset to each signal the signal is multiplied by a factor (in our case 1.1 that corresponds to 10% degradation of the signal value). The noise generated at the output is the sensitivity weight.

• $W_{distr}$ Finally the distribution weight is proposed but not used in our experiments yet. As already mentioned the distribution of the data is not absolutely uniform. If in the future the various fluctuations should be taken into account, this weight can be used to redistribute the budget among the signals with different data distributions.

### 3.2.3 Quantization Script Implementation

As indicated by the main methodology, two scripts are created to quantize the FFT. The first one quantizes the coefficients and the other the signals. The methodology suggests that the constants should be quantized first as their values are already known and they affect the signal values as well. The error budget of the FFT
block is split between the coefficients and the signals. The distribution is performed evenly (half the budget for each case) but a metric that evaluates the significance of the coefficient and the signals can be used instead.

Before getting into the details of each case a brief explanation on the calculation of the FFT is needed. To calculate the FFT a three dimensional matrix called F matrix is used. For the N-sized FFT this matrix is sized by $N \times N \times \log_2(N)$. The first two dimensions have the various coefficient placed in such a way that when the input of the FFT is multiplied by the $F(:,:,1)$ the values of the second stage are produced. Multiplying the results with the $F(:,:,2)$ gets the 3rd stage until we reach the FFT output. This method is really quick as it uses matrix multiplication (where Matlab excels) and in the same time allows as to change both the coefficients by changing the F matrix and the signals of each stage by changing the output of a multiplication. A sample F matrix for the first stage of a 8x8 FFT ($F(:,:,1)$) is shown in tables 3.1.

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Πίνακας 3.1: $F(:,:,1)$ matrix for a 8x8 FFT

### Coefficients

To quantize the coefficients the repetition concept has been used as well. The coefficients in the same stage with the same value are treated the same. However an analytical model has been developed that can calculate the noise power propagated to the output of the FFT due to the quantization of a coefficient. The formula used is the one in 3.5.
Here $F_q$ is the F matrix with the quantized coefficients. Thus the coefficient script gets as input the mean input power of the FFT intervals and the equivalent mean output power. Then by quantizing each coefficient repetition as described in the procedure above it produces the final $F_q$ matrix that is used by the signal script to calculate the FFT with quantized coefficients. In algorithm 3 the whole procedure is shown. First the normalized budget weights are computed for each repetition. Afterwards each repetition gets a solution among the Pareto solutions as described in the CSD section and the budget is redistributed among the remaining repetitions. Once all the solutions are found the final $F_{-q}$ matrix is computed, which is needed for the signals script.

**Signals**

The script that quantizes the signals is slightly different. The first major difference is that in this case no analytical model exists yet and instead of using mean power values Monte Carlo simulation is used instead.

Monte Carlo simulation is a method that uses random sampling to compute results for a system. It is usually used in non-linear or very complex systems with large number of coupled degrees of freedom that are difficult to evaluate in a different way. Monte Carlo iteratively evaluates a system's output vector for a large number of random input vectors. No single Monte Carlo method instantiation is defined in literature: the term describes a large and widely used class of approaches. However, these approaches tend to follow a particular pattern:

- **Define the domain of possible inputs** In the case of the FFT block the domain has been already defined by the the 60 GHz
Algorithm 3 Script that calculates the $F_Q$ matrix

```plaintext
procedure Coefficient_Script(error_budget,in_pow,out_pow)
  for all repetitions do
    calculate_Wsens()
  end for
  for all repetitions do
    calculate_Wrep()
  end for
  for all repetitions do
    calculate_Wstg_coef()
  end for
  for all repetitions do
    rep.budget ← rep.Wstg_coef · error_budget
    rep.pareto_options ← gen_pareto_options(rep.coef_value)
    $k ← 0$
    repeat
      $k ← k + 1$;
      $F_Q ← \text{rebuilt}_F\text{matrix}(\text{rep.pareto_options}(k))$
      degr ← calculate_noise($F_Q$)
    until degr <= rep.budget
    remaining_budget = rep.budget - degr
    redistribute_error_budget(remaining_budget)
    rep.solution ← rep.pareto_options($k$)
  end for
  for all solutions do
    $F_Q ← \text{generate}_F\text{matrix}$
  end for
end procedure
```
transceiver model. Using the model various sets of inputs are generated for different parameters such as type of transmitted data and coding used before the transmission.

- **Get sufficient number of inputs from the domain** In this case to make sure that the samples that would evaluate the FFT's output are sufficient enough their mean value has been taken into account. Samples are added to the FFT input sample set until their mean value is not changed significantly with the addition of another sample. In this case 1000 samples are sufficient for the purposes of the simulation as shown in Figure 3.12. Further increase in samples does provoke a slight change in the mean value but not a sufficiently big one that would justify the additional computational effort that is required for a single simulation.

- **Perform a deterministic computation using the inputs** Once defined for each sample in the set the FFT signals are calculated. The output of the simulation is the degradation caused due to quantization to the FFT output.

- **Aggregate the results of the individual computations into the final result** Using all 1000 outputs an average degradation is calculated for each case. This is used to compare if the available noise budget is sufficient or the quantization noise injected in the FFT is too high.

So instead of using the mean input and output power of the FFT samples as it was done in the case of the coefficient the quantized FFT for each one of the samples needs to be calculated and the mean degradation caused is the one that is taken into account to see if a quantization is valid. The signal’s script is shown in algorithm 4. Another difference is that as output we get the decimal part of the FFT repetitions (and therefore a quantization scheme of the whole FFT). The input of the script is the error budget and the FFT input samples and the output is the integer and decimal parts of the FFT signals.

The integer part of the FFT is relatively easy to calculate with the following formula (equation 3.6).
Algorithm 4 Script that calculates the DEC part of all the FFT repetitions

```
procedure Signal Script(error_budget, FFT_samples)
    for all repetitions do
        calculate_Wsens()
    end for
    for all repetitions do
        calculate_Wrep()
    end for
    for all repetitions do
        calculate_Wstg_coef()
    end for
    for all repetitions do
        calculate_INT_part()
    end for
    for all repetitions do
        rep.budget ← rep.Wstg_coef · error_budget
        rep.DECgets − rep.INT
        repeat
            DEC ← DEC + 1;
            for all FFT samples do
                calculate_quantized_FFT
                calculate_FFT_degradation
            end for
            degr ← mean_FFT_degradation
            until degr <= rep.budget
            remaining_budget = rep.budget − degr
            redistribute_error_budget(remaining_budget)
            rep.DEC ← DEC
        end for
    end procedure
```
Σχήμα 3.12: Mean value of the FFT inputs as the number of samples taken into account increase. The line shows the 1000 samples that are selected for simulation. Beyond that line the values are not fluctuating much.

\[ INT = \text{floor}(\log_2(\max(\text{abs}(\text{FFT}_{\_\text{samples}}})))) \]  

(3.6)

### 3.3 Quantization Conclusions

Many different quantization methods have been developed in the past few years. Most of the methods ([8], [9], [27], [20] and [26]) monitor the average Signal-to-Quantization Noise Ratio (SQNR) and only a few of them ([21] and [19]) monitor the maximum absolute quantization error. Although for most applications a SQNR spec is sufficient, some others may also require an upper bound on the maximum quantization error and therefore both error metrics are of interest.

All of the above methods face difficulties either in large simulation times or heavy constrains on the properties of the system under investigation. The following method proposed in [6] overcomes most
of these problems and describes a more general approach to the quantization problem. However, it still gets in CPU time problem when large algorithmic blocks with multiply-add type behaviour are present. That is for instance the case in the FFT. Hence, in this thesis we have extended this method with a major new step to remedy that weakness.

The proposed modified methodology introduces the concept of repetitions. The application of this concept heavily prunes the search space leading to a more coarse quantization of the component under investigation. As a result the quantization is not as efficient as in the case of the methodology proposed in [6] but the CPU time for quantizing the component is drastically reduced. In the case of the FFT block it has been calculated that the simulation time of the standard methodology would take up to 17500 hours to execute compared to a mere 2 hours needed by the modified method.

As far as the quality of the produced quantization scheme is concerned it is not feasible to directly compare it with the standard method but the reduction of 75% in the bits needed for representing the FFT internal signals is satisfactory. Moreover for the purposes of the experiments in chapter 4 the quantization schemes are produced using the same methodology rendering them comparable to each other. Thus the comparisons made in chapter 4 are valid.
System Scenarios in the 60 GHz Digital Baseband

4.1 Introduction to System Scenarios approach

System scenarios [15] have been recently introduced with the aim to effectively increase the energy efficiency of modern embedded systems which exhibit a large amount of dynamism. Until now a common practice to deal with the increasing complexity and the constraints of modern embedded systems was to deal separately with different use cases of a system to reduce the complexity. The concept of system scenarios groups system behaviours that are similar from multidimensional cost perspective (resource requirements, delay and energy consumption) in such a way that the system can be configured to exploit this cost similarity. Each such group is called a system scenario. Then the energy or performance of each system scenario can be separately optimized while keeping the complexity and design time acceptable.
These scenarios once identified are individually mapped on the platform during design time. During runtime a prediction mechanism detects which scenario is active and then potentially switches the system’s configuration accordingly. An enhanced mechanism can calibrate existing scenarios according to input stimuli or even create new scenarios on the fly if needed. Calibration can update the scenario definitions and both the prediction and switching mechanism.

Σχήμα 4.1: A scenario-based design flow for embedded systems.

4.1.1 Use-case scenarios versus system scenarios

In contrast to current design where a system is split in use case scenarios based on a user perspective, system scenarios further split the system in scenarios based on the system cost. Figure 4.1 depicts a design trajectory using use-case and system scenarios. It starts from a product idea, for which the stakeholders manually define the product’s functionality as use-case scenarios. These
scenarios characterize the system from a user perspective and are used as an input to the design of an embedded system that includes both software and hardware components. In order to optimize the design of the system, the detection and usage of system scenarios augments this trajectory (the bottom gray box from the figure). The run-time behaviour of the system is classified using the methodology presented in [15] into several system scenarios, with similar cost trade-offs within a scenario. For each individual scenario, more specific and aggressive design decisions can be made. In this case the FFT block is part of a use-case scenario and we break it down in system scenarios from a cost perspective, specifically the power consumption of the block.

4.1.2 Real-Time Situations

To motivate the system scenario usage in embedded system design, we start from the different Run-Time Situations (RTSs) in which a system may run on a given system platform. An RTS is a piece of system execution that is treated as a unit. Each RTS has an associated cost, which usually consists of one or several primary costs, like quality and resource usage or in the case of FFT output degradation and representation cost. Moreover, RTSs must be distinguishable from one another. Otherwise, both system situations are considered the same RTS. The system execution is a sequence of RTSs, and the current RTS is known only at the moment it occurs. In our case the RTS is fully described and distinguished from the FFT input values (FFT input interval) which consists of 512 complex signals.

However, at run time, by monitoring various system parameters (so called RTS parameters) it can be predicted in advance in which RTS the system will run next for a non-zero future time window. If the information about all possible RTSs in which a system may run is known at design-time, and the RTSs are considered in different steps of the embedded system design, a better optimized system can be built because specific and aggressive design decisions can be made for each RTS. In the current thesis the parameter used for prediction of the RTSs is based on the data correlations among the
signal waveform of the FFT input. This is a novel approach in practice, as the parameters that have been used so far for prediction in practical system scenario based methodologies, have used control variables which are more easily classified and clustered because the number of possible combinations is typically large but not exorbitant. In contrast, the data variable range is typically huge and the scenario identification step then becomes a real challenge. Because these data variables are readily available in the system behaviour their monitoring is simplified though.

Σχήμα 4.2: Design for worst case

Σχήμα 4.3: Individual mapping for each RTS.

In the traditional design approach the whole application is mapped on the architecture and scheduled in the same way. All the appli-
The other extreme would be to map each RTS individually to the architecture (Figure 4.3). Each RTS would have different access to the resources and different scheduling optimized for its needs. This would lead to maximum gain due to exploitation of RTS dynamism. But it also induces a huge overhead due to switching between the different mappings, which is far from efficient. In the case of the FFT each time the input interval changes the quantization of the signals would change, leading to locally optimal mapping with huge overhead to exploit this though.

The trade-off between these two options is the clustering of similar RTSs from a cost perspective into scenarios (Figure 4.4). Each scenario is mapped on its own way on the architecture. In this case the switching overhead is balanced out by the gain due to dynamism exploitation leading to a better optimized implementation.

For the RTS clustering a cost analysis must take place. Once we have a Pareto boundary for each one of the RTSs then the RTS with the similar cost are grouped into a scenario with the cost of the worst-case of the group. However the frequency of occurrence is taken into account too, as it is not preferable to group frequent
RTS to worse rare ones even if their costs are similar to justify such a grouping as shown in Figure 4.5.

Σχήμα 4.5: A scenario-based design flow for embedded systems.

In the case of the FFT we try to cluster its RTSs (the FFT input intervals) based on the implementation cost (related heavily also to the minimally required word-lengths).

4.2 System Scenario Methodology

The goal of a scenario method is, given a system, to exploit at design-time its possible RTSs, without getting into an explosion of detail. If the environment, the inputs, and the hardware architecture status would always be the same, then it would be possible to optimally tune the system to that particular situation. However, as stated above, since a lot of parameters are changing all the time, the system must be designed for the worst-case situation. Still, it is possible to tune the system at run-time (e.g., change the processor frequency/supply voltage), based on the actual RTS. Many system parameters exist that can be tuned at run-time while the system operates, in order to optimize the application behaviour on the platform on which it is mapped. We call these parameters system knobs.

If the knobs are fixed during run-time the system operates in the worst-case. In order to adapt the system to each scenario we need to tune the knobs. However tuning the knobs implies overhead that should be taken into account. This system scenario methodology (Figure 4.6 and the presented generic solutions for some of its steps
deal with issues that are common: choosing a good scenario set, deciding which scenario to switch to (or not to switch), using the scenario to change the system knobs, and updating the scenario set based on new information gathered at run-time. This leads to a five step methodology where each of the steps have a design-time and a run-time phase.

- **Identification of the scenario set** In this step, the relevant RTS parameters are selected and the RTSs are clustered into scenarios. For the FFT the RTS are the input intervals. The clustering is done based on a cost function. Typically this function is multi-objective but in our case we focus on the power consumption and in particular the word-length of the FFT’s internal signals. The identification step should take as much as possible into account the overhead costs introduced in the system by the following steps of the methodology. As this is not easy to achieve, an alternative solution is to refine the scenario identification (i.e., to further cluster RTSs) during these steps. The current thesis explores different RTS clustering parameters and evaluates the gains that can be achieved through such a clustering. However the number of clusters is not explored due to lack of time. Thus the number of clusters in each case is constantly 4. This number is motivated by the fact that 4 clusters introduce minor switching overhead so that the benefits of the system scenarios surpass it.

- **Prediction of the scenario** At run-time, a scenario has to be selected from the scenario set based on the actual parameter values. This selection process is referred to as scenario pre-
diction. In the general case, the parameter values may not be known before the RTS starts, so they may have to be estimated. Prediction is not a trivial task: both the number of parameters and the number of scenarios may be considerable, so a simple lookup in a list of scenarios may not be feasible. The prediction incurs a certain runtime overhead, which depends on the chosen scenario set. Therefore, the scenario set may be refined based on the prediction overhead.

As already mentioned the prediction in this scenario approach is based on the patterns of the FFT signals. A preliminary analysis on how predictable the data in the 60 GHz receiver can be was done for the digital filter and the positive results motivated to use the same approach for the FFT.

- **Exploitation of the scenario set** At design-time, the exploitation step is essentially based on some optimization that is applied when no scenario approach is applied. A scenario approach can simply be put on top of this optimization by applying the optimization to each scenario of the scenario set separately. Using the additional scenario information enables better optimization. At run-time, the exploitation is in fact the execution of the scenario. In the case of the FFT, each scenario will be characterized by different quantization schemes each one leading to different scheduling and mapping of the FFT on the ASIP. Switching between mappings is the introduced overhead and using a more efficient mapping and scheduling will lead to a more efficient implementation. In the present thesis no work is performed for actual implementation of the FFT so this step is left for future work.

- **Switching from one scenario to another** Switching is the act of changing the system from one set of knob positions to another. This implies some overhead (e.g., time and energy), which may be large (e.g., when migrating a task from one processor to another). Therefore, even when a certain scenario (different from the current one) is predicted, it is not always a good idea to switch to it, because the overhead may be larger than the gain. The switching step, selects at design-time an algorithm that is used at run-time to decide whether to switch or
not. It also introduces into the application the way to change the knob positions, that is, how to implement the switch, and refines the scenario set by taking into account switching overhead. Again the switching mechanism is not explored yet in the present thesis.

- **Calibration** The previous steps of our methodology make different choices (e.g., scenario set, prediction algorithm) at design-time that depend very much on the values that the RTS parameters typically have at run-time: it makes no sense to support a certain scenario if in practice it (almost) never occurs. To determine the typical values for the parameters, profiling augmented with static analysis can be used. However, our ability to predict the actual run-time environment, including the input data, is obviously limited. Therefore, we also foresee support for infrequent calibration at run-time, which complements all the methodology steps previously described. At design-time, information gathering mechanisms are designed and added to the application. At run-time they collect information about actual values of the parameters and the quality of the resulting system (e.g., number of deadline misses). Besides this, a calibration mechanism is introduced in the application. This is used to calibrate the cost estimates, the set of scenarios, the values of the parameters used for scenario prediction, and the knob positions. Calibration of the scenario set does not take place continuously during run-time, but only sporadically, at calibration time. Otherwise, the overhead would obviously become too large. Also note that calibration is not meaningful when quality constraints are hard. It can only be applied if constraints are soft, or to optimize average-case behaviour in the absence of constraints (e.g., when optimizing memory usage for energy reduction).

A key feature of the above methodology is that no loops are included. Once a step has been decided no need exists to revisit it later. So starting from identification all the way to calibration the methodology will calibrate an applicable scenario set as well as a prediction and switching mechanism and a calibration mechanism that can be used in run-time to further improve the system scenario imple-
4.3 Conclusions

After the generation of a different quantization scheme for each cluster the number of bits needed for representing the FFT signals have been calculated. The results are as follows: A significant gain is observed of 42% reduction on the bits needed for signal representation of the first stage of the FFT. This gain has been calculated comparing the number of bits needed when the worst case is used all the time versus the number of bits needed when the scenarios are used. So each cluster appears with a certain frequency that corresponds to the actual average behaviour.

Moreover the gain in the overall FFT has been examined and an impressive 69.4% gain is now observed. This huge difference is observed because of a steep increase in the number of bits needed in the later stages of the FFT in the case of the fourth cluster. This behaviour indicates once again that the correlation between the FFT stages should be further investigated and that the potential of the application of system scenarios on the FFT block is huge.

As far as the coefficients they are not investigated here, as motivated already in the first experiment. At present, the integer part is of not much interest either because the number of bits needed for the integer part does not fluctuate as it is saturated near the optimal value. Finally a comparison has been made between the usage of a traditional design where no quantization would take place and all signals would be set to 24 bits all the time, versus the usage of the system scenarios. An impressive reduction of 75% is observed in the number of bits needed to represent the whole FFT.

The results from the experiments show that there is a large potential of exploitation of the dynamism that is observed in the input of the FFT block. System Scenarios based on the data waveform as parameter is first put into test in this thesis and the results show that the concept can be further explored to be implemented in new more efficient designs.
Moreover the quantization procedure is proven useful as we see that the traditional design introduces a huge overhead in the actual needs of each signal. In order to reach more efficient designs a signal by signal quantization procedure should be applied in design time to remove any unnecessary bits. Reduction of the word-lengths means increased power efficiency and this can be achieved even without using the system scenario concept.
In the present thesis many innovative technologies and ideas have been explored. By combining all these innovative approaches we try to come up with more efficient system designs. In our case the potential use of the 60 GHz technology provides high data rate. And the application of the System Scenarios and the different quantization schemes provides a still very high energy efficiency, which is crucial for wireless portable systems.

5.1 Conclusions

First of all the wireless communication at 60 GHz is presented. Using the IEEE standard we propose the channel conditions that are most likely to occur in a realistic environment. We distinguish the channel modes that are most likely to be used in a commercial case as well as the channel models proposed by IEEE. With this information simulations can be set up that can provide data useful for
Moreover the potential of the Soft-SIMD processor platform is shown. The flexibility that is provided through Soft-SIMD with respect to the scheduling of an application, can lead to high-performance designs as well as less energy consumption. The potential of applying Soft-SIMD using IMEC's Feenecs ASIP template has lead to the exploration of the quantization capabilities of a hardware component. Quantization of the signals of a hardware component is not a new idea. In the current thesis we use a methodology as proposed in [6] and we extend it to fit in our needs. In order to come up with an algorithm that is feasible to use as far CPU cycles are concerned we have modified the existing methodology to reduce the complexity of the existing algorithm. To do so we have proposed a more coarse quantization that compromises the optimality of the results in an acceptable way. But it has greatly decreased the computation time, allowing us to produce multiple quantization schemes for a large hardware block such as the FFT.

Finally, we have explored the application of the System Scenarios concept based on the data of the FFT. System Scenarios represent a novel design approach that classifies the application from a cost perspective during design time and exploits the classification during run time. This way System Scenarios enable us to exploit the dynamism that is observed in a system's environment. The novelty of our approach is that the concept has not been applied before using data as parameter for classification. Most previous work uses control parameters to end up with scenarios for each system.

5.2 Future Work

In table 5.1 the outlook of the exploration space is shown. With **bold** the areas explored in the current thesis are marked. In the case of the RTS clustering (upper part of the table) as we tried only 4 clusters of the FFT input intervals we consider to have tried a coarse clustering. In the case of more clusters (a fine grain clustering), the
approach can potentially end up with more gain to the integer and the especially the decimal part.

Moreover the FFT clustering can be further explored. In our case we have used a middle case between the coarse and the fine grain quantization of the FFT block. As shown in the results of the third experiment the decimal part can be further improved in the case of a fine grain quantization of the FFT. However the computational requirements of such a calculation prohibits the use of a fine quantization. Another middle case that can lead to a finer grain quantization in acceptable computation time however should be feasible to identify.

<table>
<thead>
<tr>
<th></th>
<th>Method</th>
<th>Coarse/Fine</th>
<th>INT part</th>
<th>DEC part</th>
</tr>
</thead>
<tbody>
<tr>
<td>RTS Clustering</td>
<td>Absolute Mean</td>
<td>Coarse</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fine</td>
<td>V?</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Decimal Part Length</td>
<td>Coarse</td>
<td>X</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fine</td>
<td>V?</td>
<td>VV</td>
</tr>
<tr>
<td>FFT clustering</td>
<td>Repetitions Exploitation</td>
<td>Coarse</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Middle</td>
<td>X</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Middle</td>
<td>V</td>
<td>VV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fine</td>
<td>V</td>
<td>VV</td>
</tr>
</tbody>
</table>

Πίνακας 5.1: Outlook matrix

In Figure 5.1 the exploration space of the FFT properties and the quantization procedure is shown. As far as the FFT is concerned the space is three dimensional: it consists of time and a two-dimensional space dimensions. The time dimension consists of the different FFT input intervals or for a single FFT signal the consecutive input samples. In the current thesis this dimension has been explored through the prediction script. The data correlation on the digital filter input is promising. The prediction rate is really high and it should be explored further.

As far as the space dimensions on the one hand we have a single FFT input interval (or an interval of an internal stage of the FFT).
This is necessary to be further explored in order to find properties of the FFT inputs that can be identified and can be used for Scenario classification. The other dimension is the correlation of the data across stages. In this dimension we have to explore how a property in the first stage of the FFT propagates through the internal stages towards the output of the FFT. This is shown in the second experiment of chapter 4 when the decimal part of the last stage has been greatly reduced.

In the case of the quantization script the exploration space is divided in three subspaces. The integer part space that has to do with the reduction of the bits needed for the integer part of the signals, the decimal part which respectively has to do with the reduction of the bits of the decimal part of the signals and finally the coefficients which are represented in CSD format and therefore can be handled differently.

The exploration space of the integer part is shown in figure 5.2. In order to reduce the bits of the integer part the following can be done:

- **Fine grain quantization.** A finer grain quantization is likely to end up in a small reduction of the bits needed for the decimal part.

- **RTS clustering parameters.** Using a different parameter for
FUTURE WORK

Σχήμα 5.2: Exploration space for the integer part

clustering can potentially create clusters that exploit the dynamism observed in the integer part of the signals.

- **RTS number of clusters.** A fine grain clustering of more than four clusters can potentially end up with a gain in the bits needed for integer part even while using absolute mean value as clustering parameter.

- **Data manipulation for integer part.** A small series of experiments where the values of each stages were shifted showed us that a great potential exists to reduce the integer part through scaling. However the impact of scaling in the decimal part should be explored first.

The exploration space of the decimal part is shown in figure 5.3. In order to reduce the bits of the decimal part the following can be done:

- **Fine grain quantization.** As in the case of the integer part the decimal part can be further reduced by using a finer grain quantization. This is also shown by the results of the third experiment.

- **RTS clustering parameters.** Although the length of the decimal part as a clustering parameter has already given satisfac-
CONCLUSIONS AND FUTURE WORK

Figure 5.3: Exploration space for the decimal part

- **RTS number of clusters.** A fine grain clustering can end up with better exploitation of the dynamism of the decimal length fluctuation.

- **Data correlation across the FFT stages and signals.** As mentioned in the exploration space of the FFT properties, finding correlation across the FFT signals can lead to extracting the feature that can be used for more efficient RTS clustering as far as the decimal part is concerned.

- **Scenarios for FFT quantization stage by stage.** The further breaking of the FFT into each stages and the individual quantization of each one of them as well as the application of the System Scenario on each stage individually can potentially give great gain in the design of the block. However such approach will add a bit more switching overhead compared to the quantization of the FFT as a single block.

Finally the quantization of the coefficients is not yet explored at all in the current thesis. However the coefficients can be greatly optimized if the scheduling is taken into account. As already mentioned
in the quantization of the coefficients a gain function can be used to determine the distribution of the error budget as well as the ordering of the quantization of each coefficient.

This function in the present work takes into account only the number of ones that each coefficient needs to be represented. This factor is important but it is not the only factor that can be taken into account. When removing a '1' the distance between two consecutive ones should be taken into account. Moreover in the case that the '1' being removed is the last bit of the coefficient the gain is maximum as a whole operation is removed from scheduling. In the case that the scheduling and mapping is taken into account, the gain function should take into account the similarity between consecutive coefficients in the same loop buffer.

Finally apart from just removing a '1' while quantizing shifting of the zeros between the consecutive ones can be applied. This way the similarity of consecutive coefficients can increase as well as the values a coefficient can get making the quantization more flexible and fine grain but increasing the already huge search space.


Accuracy-guaranteed bit-width optimization.  

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